

AMENDMENTS TO THE CLAIMS:

Kindly amend claims 2, 5 and 7, and add new claim 18, as shown below.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claim 1 (previously presented): A semiconductor memory device, comprising:

a semiconductor substrate; and
gate electrodes formed for a transistor on said semiconductor substrate through a gate insulating film,
wherein a gate length of said gate electrode is longer than a half pitch.

Claim 2 (currently amended): The semiconductor memory device according to claim 1, further comprising:

a first diffusion layer formed in a surface of said semiconductor substrate to function either as one of a source [[and]] or a drain; and
a second diffusion layer formed in the surface of said semiconductor substrate to function either as the other of said source [[and]] or said drain,
wherein the shortest distance between said first diffusion layer and said second diffusion layer is proportional to said gate length.

Claim 3 (original): The semiconductor memory device according to claim 2, further comprising:

a gate insulating film formed on said semiconductor substrate and extending over said first diffusion layer and said second diffusion layer,
wherein said gate electrode is formed on said gate insulating film.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

Claim 4 (original): The semiconductor memory device according to claim 2, further comprising:

- a first insulating film provided to cover said gate electrode;
- a first contact section formed to pass through said first insulating film to said first diffusion layer;
- a bit line formed on said insulating film;
- a second contact section formed to pass through said insulating film to said second diffusion layer; and
- a capacitive section formed on said first insulating film and connected to said first contact section.

Claim 5 (currently amended): The semiconductor memory device according to claim 4, wherein a side length or diameter of said first contact section is said half pitch; and

- a side length or diameter of said second contact section [[t]] is substantially equal to said half pitch.

Claim 6 (original): The semiconductor memory device according to claim 5, further comprising:

- a second insulating film formed to cover said first insulating film, said first contact section, said second contact section and said bit line;
- wherein said capacitive section is formed on said second insulating film, and said capacitive section comprises a lower electrode, a capacitive insulating film formed on said lower electrode and an upper electrode formed on said capacitive insulating film; and
- a third contact section formed to pass through said second insulating film to said

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

first contact section.

Claim 7 (currently amended): The semiconductor memory device according to claim 1, wherein an impurity concentration of said semiconductor substrate is lower than an impurity concentration of said semiconductor substrate when the gate length of said gate electrode is substantially equal to said half pitch.

Claim 8 (previously presented): The semiconductor memory device according to claim 1, wherein the gate length of said gate electrode is equal to or longer than 1.3 times said half pitch.

Claim 9 (withdrawn): A semiconductor memory device, comprising:

a first MOS transistor formed on a first surface of a semiconductor substrate; and
a second MOS transistor formed on a second surface of said semiconductor substrate,

wherein said first MOS transistor has a first gate electrode,
said second MOS transistor has a second gate electrode, and
a gate length of said first gate electrode and a gate length of said second gate electrode are longer than a minimum processing dimension.

Claim 10 (withdrawn): The semiconductor memory device according to claim 9, wherein said first MOS transistor further comprises a first diffusion layer functioning as one of a source and a drain and a second diffusion layer functioning as the other of said source and said drain, said second MOS transistor further comprises a third diffusion layer functioning as one of said source and said drain and said second diffusion layer functioning as the other of said source and said drain,

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

—
175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

said second diffusion layer is used in common to said first MOS transistor and said second MOS transistor,

the shortest distance between said first diffusion layer and said second diffusion layer is proportional to the gate length of said first gate electrode, and

the shortest distance between said third diffusion layer and said second diffusion layer is proportional to the gate length of said second gate electrode.

Claim 11 (withdrawn): The semiconductor memory device according to claim 10, wherein said first MOS transistor further comprises a first gate insulating film extending over said first diffusion layer and said second diffusion layer,

said second MOS transistor further comprises a second gate insulating film extending over said third diffusion layer and said second diffusion layer,

said first gate electrode is formed on said first gate insulating film, and

said second gate electrode is formed on said first gate insulating film.

Claim 12 (withdrawn): The semiconductor memory device according to claim 10, further comprising:

a first insulating film formed to cover said first gate electrode and said second gate electrode;

a first contact section formed to pass through said first insulating film to said first diffusion layer;

a bit line formed on said first insulating film;

a second contact section formed to pass through said first insulating film to said second diffusion layer;

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

a third contact section formed to pass through said first insulating film to said third diffusion layer;

a first capacitive section formed on said first insulating film and connected to said first contact section; and

a second capacitive section formed on said first insulating film and connected to said third contact section.

Claim 13 (withdrawn): The semiconductor memory device according to claim 12, wherein a side length or diameter of said first contact section is said minimum processing dimension,

a side length or diameter of said second contact section is said minimum processing dimension, and

a side length or diameter of said third contact section is said minimum processing dimension.

Claim 14 (withdrawn): The semiconductor memory device according to claim 13, further comprising:

a second insulating film formed to cover said first insulating film, said first contact section, said second contact section, said third contact section and said bit line;

wherein said first capacitive section and said second capacitive section are formed on said second insulating film, and each of said first capacitive section and said second capacitive section has a lower electrode, a capacitive insulating film formed on said lower electrode and an upper electrode formed on said capacitive insulating film; and

a fourth contact section formed to pass through said second insulating film to said first contact section; and

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

a fifth contact section formed to pass through said second insulating film to said third contact section.

Claim 15 (withdrawn): The semiconductor memory device according to claim 9, wherein a gate interval between said first gate electrode and said second gate electrode is said minimum processing dimension.

Claim 16 (withdrawn): The semiconductor memory device according to claim 9, wherein an impurity concentration of said semiconductor substrate is lower than an impurity concentration of said semiconductor substrate when the gate length of said first gate electrode and the gate length of said second gate electrode are said minimum processing dimension.

Claim 17 (withdrawn): The semiconductor memory device according to claim 9, wherein the gate length of said first gate electrode and the gate length of said second gate electrode are equal to or longer than 1.3 times said minimum processing dimension.

Claim 18 (new): A semiconductor memory device, comprising:

 a semiconductor substrate;

 gate electrodes formed for a transistor on said semiconductor substrate through a gate insulating film;

 a first diffusion layer formed in a surface of said semiconductor substrate to function either as a source or a drain; and

 a second diffusion layer formed in the surface of said semiconductor substrate to function either as said source or said drain,

 wherein the shortest distance between said first diffusion layer and said second diffusion layer is greater than a half pitch.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567